IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

Determining Phase Relationships Using Digital Phase Values

Inventor(s):
Jun Kim
Michael Ching

ATTORNEY'S DOCKET NO. RB1-025US

TECHNICAL FIELD

This invention relates to clock phase synchronization and to methods of detecting clock phases.

BACKGROUND

It is often necessary to synchronize data across different clock domains. As clock frequencies increase, however, it has become more difficult to achieve the proper timing required for such synchronization.

Fig. 1 shows a typical situation that requires synchronization of an asynchronous data signal. In this example, a memory controller 10 generates a clock signal 12 that is in turn provided to a memory device 14 to coordinate data transfers. In response to clock signal 12, memory component 14 generates a data signal 16 that is in turn received by the memory controller 10. Although the data signal is generated synchronously with clock signal 12, propagation delays between the memory device 14 and memory controller 10 cause the data signal to lose synchronization by the time it reaches controller 10. Furthermore, propagation delays are different for the different memory devices of the system, so that received data signals will have different phases depending on their sources. This brings about the need for synchronization within controller 10.

Fig. 2 shows a typical prior art circuit for synchronizing a received data signal DATAIN for use with an internal clock signal CLK2. In this example, a clock source 20 generates multiple reference clock signals having known, calibrated phase relationships between each other. For example, clock source 20 might generate eight clock signals having phases that vary by 45° from each other. Clock generation circuits 22 and 23 receive the reference clock signals produce

respective clock signals CLK1 and CLK2 having phases that are specified by supplied digital phase control values PHASE1 and PHASE2.

In this example, CLK2 is the internal clock signal to which received data signals will be synchronized. CLK2 is received by the clock input of a latch or flip/flop 24 to latch the received data signal. Prior to this, however, the data signal is sampled and then synchronized by latches or flip/flops 25 and 26.

During normal operation, latch 25 is clocked by clock signal CLK1. This causes latch 25 to sample the received data signal DATAIN and to produce a captured data signal CDATA. The appropriate phase for CLK1 and the requisite digital value of PHASE1 to produce this phase are determined during an initialization procedure. During the initialization procedure, repeated attempts are made to read received data using different PHASE1 values and corresponding CLK1 phases. As a result of these attempts, a range of PHASE1 values is recorded as yielding valid results, and an intermediate one of these values is chosen for future use. During subsequent read operations, PHASE1 is set to this chosen value. Note that this setting might vary during operation, as data is received from different devices with different propagation delays.

As a result of the initialization procedure, CLK1 has an undetermined phase relationship with CLK2. Because of this, the captured data signal CDATA cannot be guaranteed to meet setup and hold times of any downstream latches or other sampling devices that are clocked by CLK2.

To ensure adequate setup and hold times at the input of latch 26, latches 26a and 26b are configured to clock CDATA either in phase with CLK2 or at 180° relative to CLK2, depending on the phase relationship of CLK2 to CLK1. Specifically, each of latches 26a and 26b receives CDATA as a data input. Latch

26a is clocked by CLK2 and Latch 26b is clocked by CLK2* (the "*" symbol is used to indicate negation or inversion). The outputs of the latches 26a and 26b are connected to the inputs of a two-to-one multiplexer 27. Depending on the value of its select input, the multiplexer presents either the clocked signal from 26a or the clocked signal from latch 26b..

The select input of multiplexer 27 receives a detect signal 30 from a phase detection circuit 31. Phase detection circuit 31 compares CLK1 and CLK2 to determine whether the phase of CLK2 relative to CLK1 is greater than 90°. If the phase is greater than 90°, detect signal 30 is asserted high to select the latched signal from latch 26a, which has been latched on the rising edge of CLK2. If the phase is less than 90°, detect signal 30 is asserted low to select the latched signal from latch 26b, which as been latched on the falling edge of CLK2.

Phase detection circuit 31 is implemented with a latch or flip/flop 32 and a signal delay element 33. Latch 32 has a clock input that receives CLK2. CLK1 is delayed 90° by delay element 33 and then provided to the data input of latch 32. This produces an output from latch 32 that is positive only if CLK2 lags CLK1 by more than 90°.

The described circuit is adequate, and has been used with success in various designs. At higher clock frequencies, however, the design effort becomes significant. Furthermore, typical delay elements (such as delay element 33) and other types of phase shifting circuits impose significant area and power requirements. Also, the phase at which the phase detection circuit triggers is fixed in the circuit described above. Therefore, it would be desirable to eliminate the need to compare clock signals to derive phase information and phase comparisons.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a memory system in accordance with the prior art.

Fig. 2 is a block diagram of a synchronization circuit in accordance with the prior art.

Fig. 3 is a block diagram showing a clock synchronization circuit in accordance with the invention.

Fig. 4 is a block diagram showing a phase detection circuit in accordance with the invention.

Fig. 5 is a block diagram showing a circuit in accordance with the invention for calibrating clocks relative to each other.

Fig. 6 is a block diagram showing a PVT detection and compensation circuit in accordance with the invention.

DETAILED DESCRIPTION

The following description sets forth specific embodiments of phase detection and synchronization circuits that incorporate elements recited in the appended claims. The embodiments are described with specificity in order to meet statutory requirements. However, the description itself is not intended to limit the scope of this patent. Rather, the inventors have contemplated that the claimed invention might also be embodied in other ways, to include different elements or combinations of storage elements similar to the ones described in this document, in conjunction with other present or future technologies.

Fig. 3 illustrates one embodiment of a clock generation and phase detection circuit 40. This circuit is useful in the context described above with reference to

Fig. 1, where a device such as a memory controller receives a bussed data signal DATAIN from a plurality of memory devices. Depending on the source of the signal, DATAIN is subject to different propagation delays as it propagates from its source to the memory controller. From any particular memory device, DATAIN will have a fixed but initially unknown phase relationship with one or more internal clock signals of the memory controller. Clock generation and phase detection circuit 40 is used within the memory controller to receive and synchronize DATAIN.

Circuit 40 includes a reference clock source 42 that generates a plurality of common reference clock signals having known, calibrated phase relationships between each other. For example, clock source 40 might generate a series of eight clock signals having phases that are 45° apart from each other.

Clock generation and phase detection circuit 40 has a plurality of clock generators that generate respective timing or clock signals. Such clock signals are derived from the reference clock signals produced by reference clock source 42. This example shows two clock generators 44 and 45. Clock generation circuits 44 and 45 in this embodiment comprise phase interpolators or phase aligners that receive the common reference clock signals from clock source 42 and interpolate between them to produce respective clock signals CLK1 and CLK2. Digital phase control values PHASE1 and PHASE2 are supplied to the clock generators to specify the desired phases of CLK1 and CLK2, respectively.

Digital phase control values PHASE1 and PHASE2 are preferably digital words, each having a number of bits that is sufficient to provide the desired phase resolution. The control values are generated by independent calibration circuits 50 and 52, using calibration procedures which will be described below.

In this example, CLK1 is used to initially sample or capture the received data signal DATAIN. CLK2 is the internal, target clock signal to which received data signals will be synchronized.

The mesochronous data signal DATAIN is received by the data input of a latch or flip/flop 47. Latch 47 is clocked or triggered by CLK1 to produce a captured data signal CDATA, which is in turn received by the data input of a latch or flip/flop 48. Latch 48 is clocked or triggered either by CLK2 or by CLK2* (as will be described in more detail below) to produce a synchronized data signal SDATA, which is in turn received by the data input of a latch 49. Finally, latch 49 is clocked or triggered by CLK2 to create an internal data signal DATA.

Calibration circuit 50 generates digital input phase control value PHASE1 to specify the phase of clock signal CLK1 relative to reference clock source 42 and to target clock signal CLK2. The value of PHASE1 and the corresponding phase of CLK1 are determined during an initialization procedure, to provide an optimum timing relationship between CLK1 and the received data signal DATAIN. The calibration or initialization procedure results in a PHASE1 value that calibrates the phase of clock signal CLK1 relative to received data signal DATAIN.

Calibration logic 50 performs this initialization by attempting to capture data signal DATAIN using a range of different PHASE1 values. This procedure identifies a subrange of PHASE1 values that result in valid data capture. An optimum value of PHASE1 is then selected from these values. For example, the optimum value might be a value in the middle of the identified subrange. Other methods of calibration might be used in other embodiments.

Calibration logic 52 is responsible for setting digital target phase control value PHASE2 and the corresponding phase of target clock signal CLK2. The value of PHASE2 can be determined by calibration logic 52 in a variety of different ways to meet the internal timing requirements of the device of which circuit 40 forms a part. For purposes of this disclosure, however, it is assumed that the phase of CLK2 is independent of the phase of CLK1 and is similarly independent of the phase of incoming data signal DATAIN. Furthermore, it is likely that the phase relationship between CLK1 and CLK2 will vary depending on a variety of factors. As an example, consider the given implementation in which DATAIN is a bus signal sourced at different times by different memory devices, each of which is a different distance from a receiving circuit 40. In an example such as this, the phase of DATAIN varies depending on which memory device is currently generating DATAIN, and the phase of CLK1 is adjusted dynamically to account for this variability. The phase of CLK2, on the other hand, is established during initialization and remains fixed thereafter. Thus, the phase relationship between CLK1 and CLK2 varies during operation, depending on the particular source of DATAIN and the propagation delays imposed on DATAIN as it propagates from the sourcing device to receiving circuit 40.

Latch 48 provides synchronization between the two mutually independent timing domains defined by CLK1 and CLK2, respectively. More specifically, latch 48 clocks the captured data signal CDATA at an appropriate timing phase to produce a synchronized data signal SDATA. Even more specifically, latch 48 is clocked either on the rising edge of CLK2 (by CLK2) or on the falling edge of CLK2 (by CLK2*). Stated alternatively, latch 48 is clocked either in phase with CLK2 or at 180° relative to the phase of CLK2. The determination of whether to

clock CDATA on rising or falling edge of CLK2 is made by considering the relative phases of CLK1 and CLK2, in a manner designed to provide adequate setup and hold times of the CDATA signal at the data input of latch 48. In further enhanced embodiments, latch 48 is clocked with one signal of a series of signals with relative phases to CLK2, such as 0°, 90°, 180° or 270°.

The determination of an appropriate phase at which to clock synchronization latch 48 is made by evaluation logic or phase detection logic 60. Rather than comparing the clock signals CLK1 and CLK2, phase detection logic 60 evaluates and compares digital control values PHASE1 and PHASE2 to detect a predetermined phase relationship between the clock signals and to determine the appropriate timing phase at which to clock captured data signal CDATA for synchronization with target clock signal CLK2.

In actual embodiment, phase detection logic 60 is an arithmetic logic unit that compares digital input phase control value PHASE1 to a reference value that represents a 90° phase offset from the target clock signal CLK2. The reference value can be expressed as REF = PHASE2 + 90, assuming that PHASE1 and PHASE2 are expressed as integers between 0 and 359. In practice, PHASE1 and PHASE2 will normally have some arbitrary range, such as between 0 and 255, where 0° is specified by a value of 0, 90° is specified by a value of 64, 180° is specified by a value of 128, and so on. In general terms, REF = PHASE2 + VAL90; where VAL90 is a value representing 90°, in accordance with the particular scale at which PHASE1 and PHASE2 are expressed relative to clock generators 44 and 45.

Phase detection logic 60 generates a detect signal 62 to indicate the result of comparing PHASE1 to the reference value. Circuit 40 includes latching logic

64 that is responsive to phase detection logic 60 and detect signal 62 to latch captured data signal CDATA at an appropriate time or phase relative to CLK2. Latching logic 62 in this embodiment comprises latch 48 in combination with a two-to-one multiplexer 66. Depending on whether detect signal 62 is true or false, multiplexer 66 supplies CLK2 or CLK2* to the clock input of latch 48.

The resulting timing is characterized as follows: if target timing signal CLK2 lags the input clock signal CLK1 by more than 90, then detect signal 62 is true, multiplexer 16 supplies CLK2 to the clock input of latch 48, and CDATA is clocked at the rising edges of CLK2; if target timing signal CLK2 lags input clock signal CLK1 by less than 90, then detect signal 62 is false, multiplexer 16 supplies CLK2* to the clock input of latch 48, and CDATA is clocked at the falling edges of CLK2. Clocking in this manner ensures that CDATA meets setup and hold requirements of latch 48, and produces a synchronized data signal SDATA that can be sampled as needed by further components operating in the time domain established by target clock signal CLK2.

The circuit of Fig. 3 effectively synchronizes data signal DATAIN across time domains, without the need to directly compare clock signals. This greatly simplifies the circuit in comparison to the prior art circuit shown in Fig. 2, by eliminating the need for a 90° delay element. In addition, the circuit of Fig. 3 can easily be used to detect and synchronize signals based on phase relationships other than 90°, simply by changing the nature of the numerical comparison performed by phase detection logic 60. Furthermore, the nature of numerical comparison by phase detection logic 60 allows more complex comparison such as with an arithmetic logic unit (ALU), look-up table, random combinatorial and/or sequential logic, etc.—phase detection logic 60 can be replaced by such different

and/or more complex logic to achieve different types of synchronization objectives.

The principles applied in the circuit of Fig. 3 can be used in other situations to detect or determine phase relationships. Fig. 4 shows one example, comprising a circuit 70 that detects the phase relationship between an internally generated reference clock signal CLKA and a received clock signal CLKIN whose phase is initially undetermined. In this example, CLKA is generated from a clock reference 71 by a clock generation circuit 72 in response to a digital phase control value PHASEA. PHASEA determines the phase of reference clock signal CLKA.

The circuit of Fig. 4 additionally includes a clock generation circuit 73 that produces a measurement clock signal CLKB having a phase that is set relative to reference clock signal CLKA by a phase control value PHASEB. PHASEA and PHASEB are preferably digital words, each having a number of bits equal to or greater than the desired phase measurement resolution.

Circuit 70 further comprises calibration logic that varies phase control value PHASEB to produce a predetermined phase relationship between measurement clock signal CLKB and received clock signal CLKIN. Specifically, the calibration logic varies phase control value PHASEB until the phase of measurement clock signal CLKB is approximately equal to the phase of received clock signal CLKIN.

The calibration logic comprises a latch or flip/flop 74 and an incrementer/decrementer 75. Latch 74 has a data input and a clock input: the data input receives clock signal CLKIN and the clock input receives measurement clock signal CLKB. This produces a detect signal 76 that is high if CLKIN leads CLKB and low if CLKIN lags CLKB.

Incrementer/decrementer 75 produces phase control value PHASEB in response to detect signal 76. Incrementer/decrementer 75 is clocked by measurement clock signal CLKB and responds by either incrementing or decrementing its digital output, depending on whether detect signal 76 is high or low. After a number of clock cycles, incrementer/decrementer 75 reaches a steady state in which its output varies by only a small amount.

Circuit 70 further comprises evaluation logic in the form of a subtraction element 77. Subtraction element 77 receives both digital control values PHASEA and PHASEB, and in response produces a digital, multi-bit value indicating the numerical difference PHASEA/B between PHASEA and PHASEB. This value corresponds to the phase difference between CLKA and CLKB. Because PHASEB has been adjusted to make the PHASE of CLKB equal to that of received clock signal CLKIN, PHASEA/B also represents the difference in phase between CLKIN and reference clock signal CLKA.

Fig. 5 illustrates yet another application of phase detection using the concepts already discussed. Fig. 5 shows a plurality of clock generation circuits 84 that generate respective clock signals CLKA, CLKB, CLKC, and CLKD in response to digital control values PHA, PHB, PHC, and PHD. The digital control values specify desired relative phases of the clock signals, as described above. The generated clock signals are based on or derived from a common clock reference 85, which supplies one or more common reference clock signals as discussed above.

The clock signals are buffered by elements 86, which subject the clock signals to different propagation delays. The circuit includes calibration logic 88 that adjusts or corrects the digital control values to account for the different

propagation delays. Specifically, the calibration logic 88 receives digital control values PHASEA, PHASEB, PHASEC, and PHASED that indicate the desired phases of the clock signals. The calibration circuit has adjustment blocks 90 that add an appropriate correction value to each supplied control value PHASEA, PHASEB, PHASEC, and PHASED, producing the control values PHA, PHB, PHC, and PHD that are supplied to clock generators 84.

The calibration logic 88 performs an initialization or calibration procedure to determine the appropriate correction values for the respective digital control values. The initialization procedure comprises varying digital control values PHASEA, PHASEB, PHASEC, and PHASED to produce a predetermined phase relationship between the clock signals. More specifically, the calibration logic varies digital control values PHASEA, PHASEB, PHASEC, and PHASED so that the buffered clock signals CLKA, CLKB, CLKC, and CLKD have approximately identical phases. The calibration logic then derives correction values from the digital control values PHASEA, PHASEB, PHASEC, and PHASED that produce such phase alignment. Generally, the correction values comprise the differences between the control values that produce phase alignment. Normally, one of the clock signals will be designated as a reference, and the differences will be calculated with respect to the control value corresponding to the reference.

Subsequent to the initialization procedure, digital control values PHASEA, PHASEB, PHASEC, and PHASED are supplied by other circuits. Calibration logic 88 then compensates these control values with the derived correction values to produce compensated phase control values PHA, PHB, PHC, and PHD, to account for the different propagation delays of the clock signals CLKA, CLKB, CLKC, and CLKD.

Fig. 6 shows another application of comparing digital phase control values, in this case to adjust for PVT variations. This example circuit 100 includes a PVT-sensitive circuit 102 that is sensitive to PVT (process, voltage, and temperature) variations. As an example, PVT-sensitive circuit 102 might comprise a driver that produces an output signal whose slew rate is sensitive to PVT variations. In some circuits, it is highly desirable to maintain a constant slew rate. Accordingly, it becomes necessary in such circuits to compensate for PVT variations in order to maintain the constant slew rate.

Circuit 100 includes two clock generators 104 and 105 that derive clock signals CLKA and CLKB from a clock reference 106. The relative phases of the clocks are established in the manner described above by digital phase control values PHASEA and PHASEB. In this example, clock signal CLKA acts as a fixed reference while PHASEB is varied to vary the phase of clock signal CLKB relative to that of CLKA.

The circuit includes a delay element 108. This delay element is designed and configured to delay clock signal CLKB by a phase delay that varies with PVT variations. The delay element produces a delayed clock signal CLKC.

Both CLKA and CLKC are provided to calibration logic 110. In a calibration procedure that is repeated periodically, logic 110 varies phase control value PHASEB to find a value of PHASEB that produces a predetermined phase relationship between delayed measurement clock signal CLKC and reference clock signal CLKA. More specifically, logic 110 finds a value of PHASEB that produces a CLKC phase that is approximately equal to that of reference clock signal CLKA. In an arithmetic element 112, this value of PHASEB is subtracted from PHASEA to yield a PVT adjustment value PVTADJ, which is in turn

provided to PVT-sensitive circuit 102. PVT-sensitive circuit 102 is configured to compensate as necessary for changes in PVTADJ, thereby maintaining constant functionality regardless of PVT changes.

In the example embodiments disclosed above, clock signals are described and shown as being generated in response to digital control words. However, it may alternatively be the case that some or all of the clock signals in a particular circuit are generated by other means (such as by analog clock generators), with corresponding digital control words being generated by phase detection circuitry. The circuits and techniques described above are equally applicable in situations such as this, in which the various comparison techniques will be applied to the digital control words generated by the phase detection circuitry.

Although details of specific implementations and embodiments are described above, such details are intended to satisfy statutory disclosure obligations rather than to limit the scope of the following claims. Thus, the invention as defined by the claims is not limited to the specific features described above. Rather, the invention is claimed in any of its forms or modifications that fall within the proper scope of the appended claims, appropriately interpreted in accordance with the doctrine of equivalents.